Technical Examination Board, Gujarat State, Gandhinagar

Foundation Course in VLSI Design

Title	ESDM106:Foundation Course in VLSI Design
Level	Certificate Course
Course Duration	Four Month (Part time) Two Week (Full Time) 90 Hrs (Th. 30 Hrs Pr. 60 Hrs)
Entry Qualification	B.E./B.Tech/Diploma/B.E. Sem.III onward/ Diploma Sem. IV onward (EC/IC/IT/CE or Similar Branch)/ BCA/MCA/B.Sc./M.Sc./Any other graduate(with Physics/IT)

Teaching Scheme:

Sub Code	Subject Name	Teaching Scheme		Examination Scheme				Term Work Marks	Total Marks
		Theory	Practical	Theory Marks	Hrs.	Practical Marks	Hrs.		
ESDM106	Foundation Course in VLSI Design	2	4	50	2	100	4	25	175

Total Week	= 15	Theory	= 1 hour slot
Total Teaching slot/Week	= 04	Practical	= 2 hour slot
Theory Periods	= 30	Total teaching	
Practical Periods	= 60	06 hours/week (Part-time) 06 hours/day (Full time)	

ESDM106: Foundation Course in VLSI Design

VLSI Design has become more and more common as a core technology used to build electronic systems. By integrating soft-core or hard-core processors, these devices have become complete systems on a chip, steadily displacing general-purpose processors and ASICs. In particular, high-performance systems are now almost always implemented with FPGAs. As per the recently published data, there are over 20,000 engineering professionals working in more than 150 companies in the chip designing industry and there is a huge demand for high-quality trained manpower in this field. This program will enhance the career opportunities of the participants in upskilling/reskilling in Verilog hardware description language (HDL) and its use in programmable logic design. The emphasis is on the synthesis constructs of Verilog HDL; however, it will enable the participant to use FPGA architecture for a given application along with practical design skills state of the art software tools for FPGA development, and solve critical digital design problems implemented in FPGAs to achieve industry level design skills.

Course Objectives:

After successful completion of this Course, students will be able to:

- Understand brief history, present and future and Design Cycle of VLSI technology. Understand the Design Cycle of VLSI.
- Understand Verilog programming syntax. Level of Abstraction in Verilog programing writing and simulating test benches in Verilog.
- Design and Develop IPs for VLSI using Verilog HDL.
- Emulate, debug & Characterize reusable IPs.

ESDM106 : Foundation Course in VLSI Design	
Unit-1	**Course in VLSI Design**
1.1	Number System
1.2	Logic Gates
1.3	Latches and Flip Flops
1.4	Combinational Logic Circuit
1.5	Sequential Logic Circuit
Out come	Basic athematic operation using binary numbers and the conversion. Understanding of different types of gates and building logical circuit using basics and universal gates. Knowledge of different types of flip-flop and latches and operation of combination and sequential circuit
Unit -2	**Basics of Digital VLSI Technology**
2.1	Basics of Digital VLSI Technology Historical Perspective. VLSI technology trends.
2.2	Performance measures and Moore's law comparisons of technology trends. Introduction to the family of Transistor.
2.3	Basics of CMOS Transistor. MOSFET Fabrication Process
2.4	VLSI Design Flow, Introduction to ASIC & FPGA
Out come	Understand brief history, present and future and Design Cycle of VLSI technology. Understand the Design Cycle of VLSI.
Unit -3	**Fabrication Process and Layout Design Rules**
3.1	Fabrication Process and Layout Design Rules
3.2	Introduction to fabrication Process.
3.3	General Aspects of CMOS Technology.
3.4	CMOS Inverter Fabrication Process, Layout Design Rules.
3.5	Semi-Custom Design Flow, Full-Custom Design Flow
Out come	Understand Layout Design Rules. Working principal, structure and operation of transistors like NMOS, PMOS and CMOS. Understanding of fabrication Process MOSFET and CMOS devices.
Unit -4	**Digital CMOS Design**
4.1	CMOS Inverter Basics.
4.2	Inverter Transfer Characteristics, Inverter sizing.
4.3	Inverter Design
4.4	Other types of Inverter and its problem.
Out come	Understand the Digital CMOS Design. Design CMOS Inverter and analyze transfer characteristics. Types of inverter, their problem and solutions.

Unit -5	Hardware Modeling Using Verilog
5.1	Introduction to Verilog and Programming Structure
5.2	Level of Abstraction Data Type
5.3	Behavioral Modeling and Timing
5.4	Verilog Procedural Assignment
5.5	Introduction to Blocking Non-Blocking Assignments in Verilog
5.6	Verilog Functions, Verilog User Defined, Primitives
5.7	Writing Very First Program, Writing Test Benches in Verilog, Verilog Simulation Basics
Out come	Writing and simulating small programs and test benches in Verilog
Unit -6	**Implementation and Simulation of Logic gates/circuits in Verilog**
6.1	Implementation of Logic Gates using Dataflow modeling in Verilog
6.2	Implementation of Universal Gates using Dataflow modeling in Verilog
6.3	Implementation of Logic Gates using Gate-Level modeling in Verilog
6.4	Implementation of Universal Gates using Gate-Level modelling in Verilog
6.5	Implementation Mux in Verilog
6.6	Implementation different flip- flops in Verilog
6.7	Implementation Combinational Logic Circuit in Verilog
6.8	Implementation Sequential Logic Circuit in Verilog
Out come	Implementation and Simulations of Basic, universal Gates using different modelling in Verilog Implementation and Simulations of Mux (2:1, 4:1,8:1) in Verilog. Implementation and Simulations of Combinational and Sequential in Verilog

Suggested List of Practical's

Sr. No	Practical Name
1	Study different types of gates and building logical circuit using basics and universal gates.
2	Study design Cycle of VLSI.
3	Design CMOS Inverter and analyze transfer characteristics.
4	Simulate various programs and test benches in Verilog.
5	Simulate Combinational and Sequential circuits in Verilog.

Course Reference: (Short Term Courses – NIELIT, GoI)